CLAIMS

WHAT IS CLAIMED IS:

1. A digital data-transmission system for the transmission of digital audio data, comprising:

a transmitting arrangement comprising

a first signal processing circuit (12) coupled to the output of said analog/digital converter (10) for converting the signal shape of said digital data signals to a signal shape that can be transmitted loss-free;

a transmitter (11) coupled to the output of said first signal processing circuit (12) for transmitting the converted digital data signals; and,

a receiving arrangement for reconverting the data signals received from said transmitter (11).

2. The digital data-transmission system according to claim 1 wherein said receiving arrangement comprises:
a receiver (50), a second signal-processing circuit (55), coupled to the output of said receiver (50) for recovering from the received digital data signals, a digital data signal

with a signal shape analogous to that of the original data signal of said transmitting arrangement.

3. The digital data-transmission system according to claim 2 wherein said transmitter (11) and said receiver (50) communicate wirelessly.

4. The digital data-transmission system according to claim 3 wherein said transmitter (11) and said receiver (50) communicate via a fiber optic line.

5. The digital data-transmission system according to claim 3 wherein said transmitter (11) and said receiver (50) communicate via antennas (11a, 51).

6. The digital data-transmission system according to claim 5 wherein said antennas (11a, 51) are directional radio antennas.

7. The digital data-transmission system according to claim 1 wherein the transmission frequency lies in the GHz region and in particular is 2.465 GHz.

8. The digital data-transmission system according to claim 7 wherein the transmission frequency lies in the MHz region and in particular is 868 MHz.

9. The digital data-transmission system according to claim 1 wherein the signal-shape processing comprises an amplitude processing.

10. The digital data-transmission system according to claim 9 wherein the signal amplitude is adapted to TTL level.

11. The digital data-transmission system according to claim 1 wherein said first signal processing circuit processes the signal edges of said digital data signals.

12. The digital data-transmission system according to claim 11 wherein said digital data signals are trapezoidal data-stream signals, wherein the steepness of the signal edges is increased.

13. The digital data-transmission system according to claim 12 wherein the data signal is converted into a rectangular signal.

14. The digital data-transmission system according to claim 2 wherein said first signal-processing circuit (12) at the transmitter end is clocked by a clock signal (WLCK, LRCK) of the original digital data signal.

15. The digital data-transmission system according to claim 1 wherein said second signal-processing circuit (55) at the receiver end is clocked by a clock (LRCK) of the digital data stream output.

16. The digital data-transmission system according to of claim 1 comprising an A/D converter (10) coupled as the input stage to said first signal processing circuit of said transmitting arrangement, wherein said first processing circuit (12) is clocked by clock signals (WLCK, LRCK) of said A/D converter (10).

17. The digital data-transmission system according to claim 16 wherein said first processing circuit (12) of said transmitting arrangement comprises a flip-flop circuit (26) for processing the amplitude of the digital data signals from said A/D converter (10) to said transmitter (11).

18. The digital data-transmission system according to claim 16 wherein said first processing circuit (12) at said

transmitter end comprises a NAND gate circuit (29) for processing of the edge steepness of the digital data signal from said A/D converter (10) to said transmitter (11).

19. The digital data-transmission system according to claim 16 comprising a buffer circuit (18) connected to the output of said A/D converter (10).

20. The digital data-transmission system according to claim 17 wherein said first processing circuit (12) at said transmitting arrangement comprises an inverter circuit (34) coupled to its output for serial output of the data of the digital data signal from said signal-modification circuits (26, 29).

21. The digital data-transmission system according to claim 16 wherein said first processing circuit (12) at the transmitter end comprises a buffer circuit (40) as the output stage.

22. The digital data-transmission system according to claim 21 comprising an amplitude-trimming circuit (46) connected to the output of said buffer circuit (40).

23. The digital data-transmission system according to claim 16 comprising a D/A converter (52) as the output stage at the receiving arrangement wherein the signal processing function of said second processing circuit (55) of the receiver end is designed to be complementary to said first processing circuit (12) of said transmitting arrangement.

24. The digital data-transmission system according to claim 23 wherein said second processing circuit (55) of said receiving end arrangement is clocked by clock signals (LRCK) of said D/A converter (52).

25. The digital data-transmission system according to claim 23 wherein said second processing circuit (55) of said receiving arrangement comprises a flip-flop circuit (65) for recovery of the amplitude of the original digital data stream supplied by said A/D converter from the digital data signal supplied by said receiver (50).

26. The digital data-transmission system according to claim 23 wherein said second processing circuit (55) of said receiving arrangement comprises a NAND gate circuit (69) for recovery of the edge steepness of the original digital data signal from the digital data signal of said receiver (50).

27. The digital data-transmission system according to claim 23 comprising a buffer circuit (59) connected to the output of said receiver (50).

28. The digital data-transmission system according to claim 27 comprising an amplitude-trimming circuit (56) connected at the input of said buffer circuit (59).

29. The digital data-transmission system according to claim 23 wherein said second processing circuit (55) of said receiving arrangement comprises an inverter circuit (74), connected to the input of said D/A converter (52), for serial output of the data of the digital data signal.

30. The digital data-transmission system according to claim 23 wherein said second processing circuit (55) of said receiving arrangement comprises a buffer circuit (87) serving as the output stage.

31. The digital data-transmission system according to claim 30 comprising an amplitude-trimming circuit (79) connected to the input of said buffer circuit (87).

32. The digital data-transmission system according to claim 1 wherein the digital data signal is organized into a

number of $n > 2$ channels, in said transmitting arrangement, and multiplexed by means of a digital multiplexer on a bus system, which is interconnected to said first processing circuit (12) of said transmitting arrangement.